IDEC Chip Design Contest

Closed-Loop Neural Interface Available Simultaneously Recording and Stimulation using Fast Convergence Stimulation Artifact Removal

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Abstract

The closed-loop neural interface has serious issue that stimulation itself make huge artifacts (~mV) in recording system saturating amplifier, contaminating bio-signal (~ 50μV) and the post-analysis during disturbed period. Several stimulation artifact removal (SAR) techniques have trade-off between conversion time and algorithm accuracy. Here, we suggested closed-loop neural interface using fast convergence SAR algorithm while sustaining adequate removal accuracy. The amplifier-free ADC-direct 2nd-order continuous delta-sigma modulator recording stage is adopted to provide ~15μVrms input-referred integrated noise from 5Hz to 5kHz which is adequate to record bio-signal. It succeeds to record ~10mV signal about the size of stimulation artifact. The fast-convergence SAR module provides stable accuracy under versatile recording environment. The chip is designed using TSMC 65-nm CMOS process. The Chip is composed of 18 input channels, 2 SAR block, 1 stimulation channel and 2 CIC Filter for down-sampling. The Entire chip area is 1mm^2.

Design & Measurement

Biopotential Sensor Design

Each input channel has a dedicated 2nd-order Delta-Sigma Modulator (DSM) ADC-direct configuration [1]. Input is chopped at f_{ch} to segregate flicker noise from input signal band. A 1bit quantizer compare integrated errors at f_{chop}. Using output of quantizer (D) digital auto-ranging and prediction module controls the size of LSB of quantizer and predicts input signal (P). P is chopped and feedbacked to input side through a 12-bit Capacitive Digital to Analog Convertor (CDAC). Error signal re-enters to analog integrator and cycles feedback loop.

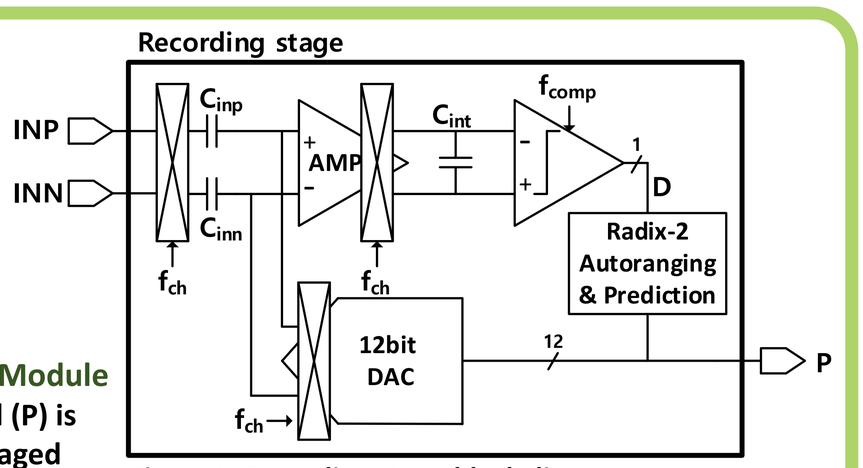

Figure 1. Recording stage block diagram

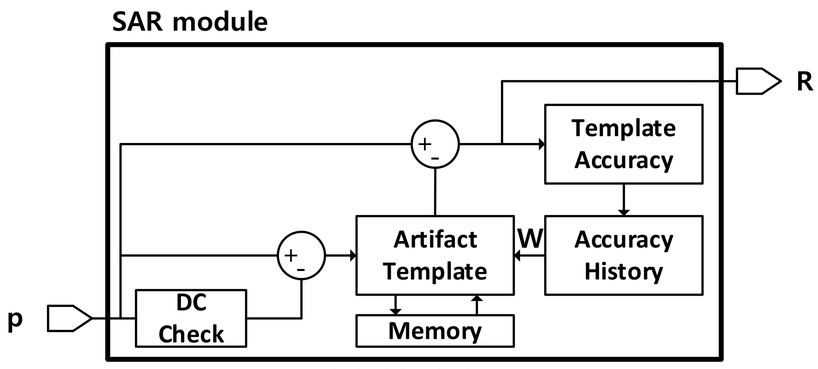

Figure 2. SAR module block diagram

Signal Data Flow

Input is predicted by recording stage and predicted signal (P) is artifact removed (R). R passes CIC filter for the final output and enters feature extractor to determine target situation. Stimulation control signal (C) inform SAR module and stimulator the timing of stimulation.

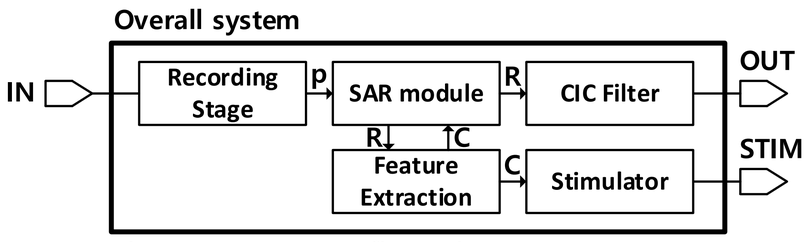

Figure 3. System configuration

Stimulation Artifact Removal Module

Contaminated prediction signal (P) is DC-canceled and weighted averaged to generate artifact template based on weighting factor (W). P is subtracted by template signal and produces recovered clean signal (R). By checking R, template accuracy check module determines the size of residue artifact and control W for next learning cycle. R will pass through CIC filter for down-sampling and low pass filtering to make the final output.

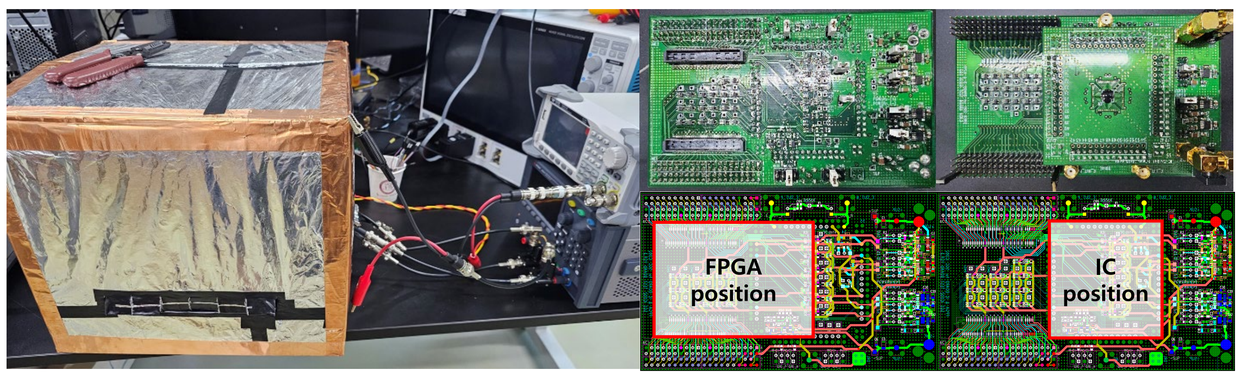

Figure 4. Measurement setup

Measurement

Chip board is placed inside the handmade faraday box to prevent interference from outer noise. Right above shows PCB test bench. The left one shows FPGA connector part and the right one shows IC connector part. Each parts is on the opposite site of the PCB test bench. Fake stimulation artifact data is injected inside the chip using SPI module for the SAR test.

Result & Conclusion

Result

Chip input referred noise is tested using low noise 1mVpp 316Hz sine wave signal. Calculated input referred noise is about 15μVrms from 5Hz to 5kHz range (fig 5. (A)) which is enough to record bio-signal like LFP (~500Hz signal band), action potential (~ 5kHz signal band). It shows that designed IC is succeed to record ~mV range signal under that noise condition and possible to record stimulation artifact and bio-signals at the same time. To test SAR function fake stimulation artifact data is injected using SPI module inside the chip. Fig 5. (B) shows that about 3mVpp of stimulation artifact data is reduced into ~150μVpp about 60dB rejection quality while maintaining recording data.

Conclusion

In this work, overall system achieves 15μVrms IRN in 5 ~ 5kHz, record ~mV of signal and reject about 60dB of artifact. It can be used to control neural system.

Performance	This work	[2]	[3]
Process	65nm CMOS	65nm CMOS	Sub-μ CMOS
Supply voltage (V)	1 / 2	1.2 / 2.5	5.25
Artifact Suppression (dB)	60	60	100
Input referred noise (nV/√Hz)	296.8	126.9[2]	144.6
Artifact rejection delay	< 1s [1]	< 2s	-[3]

Table 1. Comparison Table

[1] At 100Hz stimulation frequency
[2] Calculated from table in [13]
[3] Conducted on external device

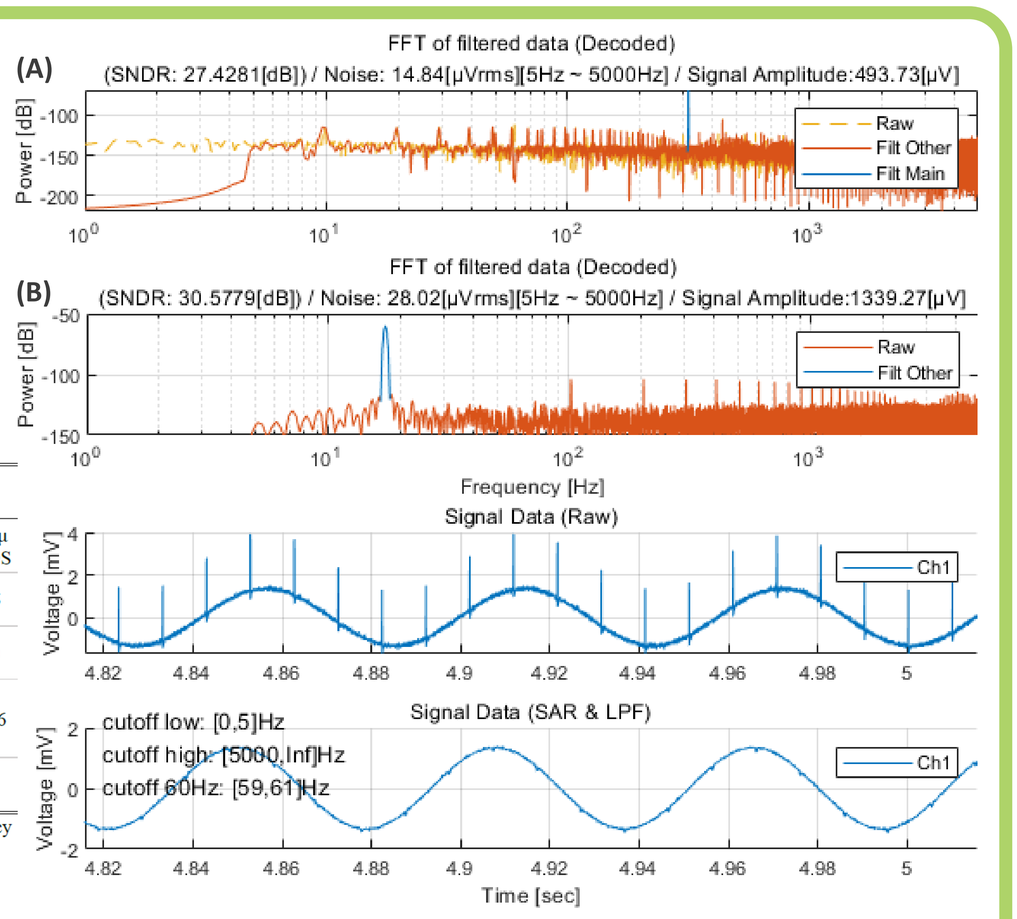

Figure 5. Test Result: (A) Input referred noise; (B) SAR accuracy

Reference

[1] 조재욱, *et al.*, JICAS, 2023.
[2] Uehlin, J. P., *et al.*, JSSC, 2020.
[3] Culaclii, *et al.*, TBioCAS, 2018.

Acknowledgement

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